according to the present invention and is similar with the second method shown in Fig.12. In the third method, a plurality of photoresists 72 is generated by exposing with different degrees of decomposition on the semiconductor wafer 30 twice. Three groups of photoresists 72, completely dissolved, undissolved and partly dissolved, are formed on the surface of semiconductor wafer 30 and are used as masks when etching. As shown in Fig.13, the method requires being exposed twice. First, a plurality of undissolved photoresists 72 are applied to the surface of semiconductor wafer 30 by using an optical mask 70 with areas with light penetration capability of 100% (the space parts) and areas with light penetration capability of 0% (the parts with oblique lines). Next, the photoresists 74 that determine the positions of dummies and new shallow trenches are partly dissolved by using another optical mask 80 (as shown Fig.14) comprising both areas with light penetration capability of 100% (the space parts) and 0% (the parts with oblique lines). After etching, the semiconductor wafer 30 with a plurality of dummies and shallow trenches as shown in Fig.11 is made.

In the claims:

1. (Once amended) A method for electrically isolating shallow trenches between components on the surface of a semiconductor wafer comprising:

(a) forming a plurality of first-type trenches and second-type trenches on a semiconductor substrate, each of the first-type trenches having a width greater than a predetermined size

that is greater than a width of each of the second-type trenches;

(b) performing a photolithographic process to form at least one photoresist pattern in each of the first-type trenches;

(c) performing an etching process to form at least one dummy and a plurality of third-type trenches in each of the first-type trenches with the photoresist patterns as masks, and to deepen each of the second-type trenches;

B3

(d) stripping the photoresist patterns;

(e) forming a dielectric layer over the surface of the semiconductor wafer, wherein the dielectric material of the dielectric layer fills the first-type trenches, the second-type trenches, and the third-type trenches on the surface of the semiconductor wafer;

(f) condensing the dielectric layer; and

(g) performing a planarization process to polish the surface of the semiconductor wafer for aligning the surface of the dielectric layer inside each of the first-type trenches and the second-type trenches with the surface of each component on the semiconductor wafer.

2. (Once amended) The shallow trench isolation method of claim 1 wherein the predetermined size is about 2 μm.

5. (Once amended) The shallow trench isolation method of claim 1 wherein each component on the semiconductor wafer surface comprises a Si substrate, a pad oxide

B4

layer above the Si substrate, and a pad nitride layer above the pad oxide layer, and the planarization process performed on the dielectric layer surface makes this surface inside each of the first-type trenches and the second-type trenches align approximately with the pad nitride layer of each component on the semiconductor wafer surface; wherein the shallow trench isolation method further comprises:

performing a second planarization process to strip off the pad oxide layer and pad nitride layer from each component, and make the surface of the dielectric layer inside each of the first-type trenches and the second-type trenches approximately align with the surface of the Si substrate of each component.

B4

6. (Once amended) The shallow trench isolation method of claim 5 wherein the bottom of each of the first-type trenches and the second-type trenches on the semiconductor wafer is formed by a Si substrate, and each dummy is also made of Si.

7. (Once amended) The shallow trench isolation method of claim 6 wherein after the second planarization process, the dielectric material formed in each of the first-type trenches remains covered over each Si dummy for electrical isolation.

12. (Once amended) The shallow trench isolation method of claim 1 wherein each dummy is formed at the bottom of each of the first-type trenches.

B5

Rule 1.126

13. (Canceled)

20~~14~~. (New) A method for forming electrically isolating shallow trenches between components on the surface of a semiconductor wafer comprising:

(a) providing a semiconductor substrate having at least a first-type trench region used to form a first-type trench, and a second-type trench region used to form a second-type trench, the first-type trench having a width greater than a predetermined value that is greater than a width of the second-type trench;

(b) forming a first photoresist pattern on the semiconductor substrate exposing the first-type trench region and the second-type trench region, and at least a second photoresist pattern on the first-type trench region, the second photoresist pattern having a smaller height than the first photoresist pattern;

B6

(c) etching the first-type trench region and the second-type trench region to form the first-type trench and the second-type trench with the first photoresist pattern as a mask, and to form at least one dummy at a bottom of the first-type trench with the second photoresist pattern as a mask;

(d) stripping the first photoresist pattern and the second photoresist pattern;

(e) forming a dielectric layer over the surface of the semiconductor substrate, wherein the dielectric material of the dielectric layer fills the first-type trench and the second-type

trench on the surface of the semiconductor substrate;

(f) condensing the dielectric layer; and

(g) performing a planarization process to polish the surface of the semiconductor wafer for aligning the surface of the dielectric layer inside each of the first-type trench and the second-type trench with the surface of each component on the semiconductor substrate.

21 20
15. (New) The method of claim ~~14~~ further comprising:

forming a photoresist layer over the semiconductor wafer; and

utilizing an optical mask of different sets of light penetration capability to perform a photolithography process on the photoresist layer for simultaneously forming the first photorsist pattern and the second photoresist pattern in the photoresist layer.

B6

22 21
16. (New) The method of claim ~~14~~ further comprising:

forming a photoresist layer over the semiconductor wafer;

exposing the photoresist layer to light through a first optical mask of different sets of light penetration capability to define the first photorsist pattern;

exposing the photoresist layer to light through a second optical mask of different sets of light penetration capability to define the second photoresist pattern; and

developing the photoresist layer to form the

first photorsist pattern and the second pattern.

23 20
17. (New) The method of claim ~~14~~ wherein the predetermined value is about 2 μm.

BO

5

24 20
18. (New) The method of claim ~~14~~ wherein a preferred height of any dummy is around 300 Å to 500 Å.